JESD204A for wireless base station and radar systems

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0.0 Introduction - New trends for wireless base station and radar systems

Digital Signal Processing (DSP) technology continues to transform radar systems and wireless cellular Base Transceiver Station (BTS) systems. DSP technology has made possible the dramatic gains in radar sensitivity, range and image quality, as well as the gains in the cell phone radio performance, data bandwidth and power efficiency. Next generation radar and BTS systems continue to leverage advancing DSP technology with advanced techniques including synthetic beam forming and beam steering.

1.0 Characteristics of beam forming/beam steering AESA radar and radio BTS system designs

Synthetic beam forming and beam steering systems typically use one-dimensional (linear array) or two-dimensional (matrix array) transceiver (TRx) antenna array elements. In so-called Active Electronically Scanned Array (AESA) radar systems, there may be hundreds or even thousands of such elements in the array. Each transmit exciter and receiver element connects to a DSP or a DSP farm, where the data processing computing element may be a programmable DSP chip, an ASSP, or a FPGA. Using algorithms developed years earlier, but only made practical with today's low-cost hardware, the DSP engines scan the array, and apply complex (magnitude and phase) filter functions to the incoming Rx and outgoing Tx data streams to create a synthetically focused beam to enhance the Rx and Tx performance. In the case of radar, this technique eliminates traditional mechanical scanning, and enables highly agile target acquisition. Because the beam is synthetically derived from the antenna element data streams, multiple beams can be formed and steered on one array, up to the computing power limits of the DSP. This allows multiple targets to be acquired and tracked simultaneously.

An analogous situation exists in the case of BTS, especially in OFDM systems such as WiMAX and LTE. A linear array of antenna elements uses similar DSP algorithms to form a beam for each subscriber mobile radio, and adaptive beam forming allows for power-efficient tracking of the subscriber radio, while minimizing interference in adjacent radios. Adaptive beam forming offers enhanced range/sensitivity, interference immunity, and power efficiency compared to conventional antenna and digital baseband processing technologies.

Beam forming technology requires high processing bandwidth, with computational speeds approaching several billion Multiply And Accumulate (MAC) operations per second. Such computationally demanding applications quickly exhaust the processing capabilities of conventional digital signal processing chips. FPGAs, with embedded DSP blocks and high throughput memory subsystems, provide a high-performance platform for beam forming applications.

2.0 Trends in FPGAs and high speed data converters (SERDES-based interfaces, JESD204A)

The current generation of FPGAs offer enormous DSP performance, far beyond the performance capability of traditional digital signal microprocessors. For example, the Altera Stratix V FPGA family offers up to 1840 G MACS and 1000 G FLOPS algorithmic performance and as many as 66 high speed SERDES channels. These FPGAs also offer high bandwidth SERDES-based serial interfaces which are the only practical method of interconnecting the FPGA to the array element data converters. Note that each array element can produce [Rx] or consume [Tx] hundreds of megabytes of data per second.

3.0 Merits of JESD204A in beam steering system designs – rate, reach, interoperability

Fortunately, there is a new data converter interface, called JEDEC JESD204A, that makes the implementation of beam forming/steering systems cost effective. This data converter interface specifies one or several high speed serial data lanes operating at up to 3.125 Gbit/s. The NXP Semiconductors' CGV implementation of this standard runs at up to 4.0 Gbit/s, with a 100 cm typical reach. Altera and NXP have collaborated on interoperability testing to ensure "plug and play" interworking of the Altera JESD204A transmit and receive IP blocks with the NXP ADCs and DACs.

Table 1 shows some of the key elements of the different versions of JEDEC JESD204.

Table 1. Evolution of JESD204 specification

Function	JESD204	JESD204A	JESD204B[1]
JEDEC specification release	2006	2008	2011
Maximum lane rate (Gbit/s)	3.125	3.125	6.25
Support for multiple lanes?	no	yes	yes
Support for lane synchronisation?	no	yes	yes
Support for deterministic latency?	no	no	yes
Support for harmonic clocking?	no	no	yes

[1] Expected in JESD204B.

There are numerous system design merits associated with JESD204A compared to legacy parallel interfaces. These benefits include:

- fewer higher bandwidth interconnect PCB traces, enabling higher reliability systems (most failures occur at points of interconnect)
- reduced PCB complexity, which impacts both NRE costs and marginal costs as the system can very often be implemented using fewer PCB layers
- opening up of a critical bottleneck in the signal processing bandwidth of the system design

4.0 Two system design examples

Figure 1 shows how JESD204A enables cost-effective phased array TRx systems. Because of the high DSP capacity of the Stratix V family, each FPGA can service the data streams of several TRx array elements. The 100 cm reach of NXP's CGV converters enables considerable system mechanical design flexibility. FPGA SERDES channels can be used to interconnect FPGAs in a star network or other multiprocessing network topology. Note that inexpensive, low-power FPGAs, such as the Altera Cyclone and Arria families (which include SERDES I/O resources) can be used as JESD204A signal repeaters to extend the run length of the differential data lanes, aggregate JESD204A data lanes, and accommodate physically large arrays.

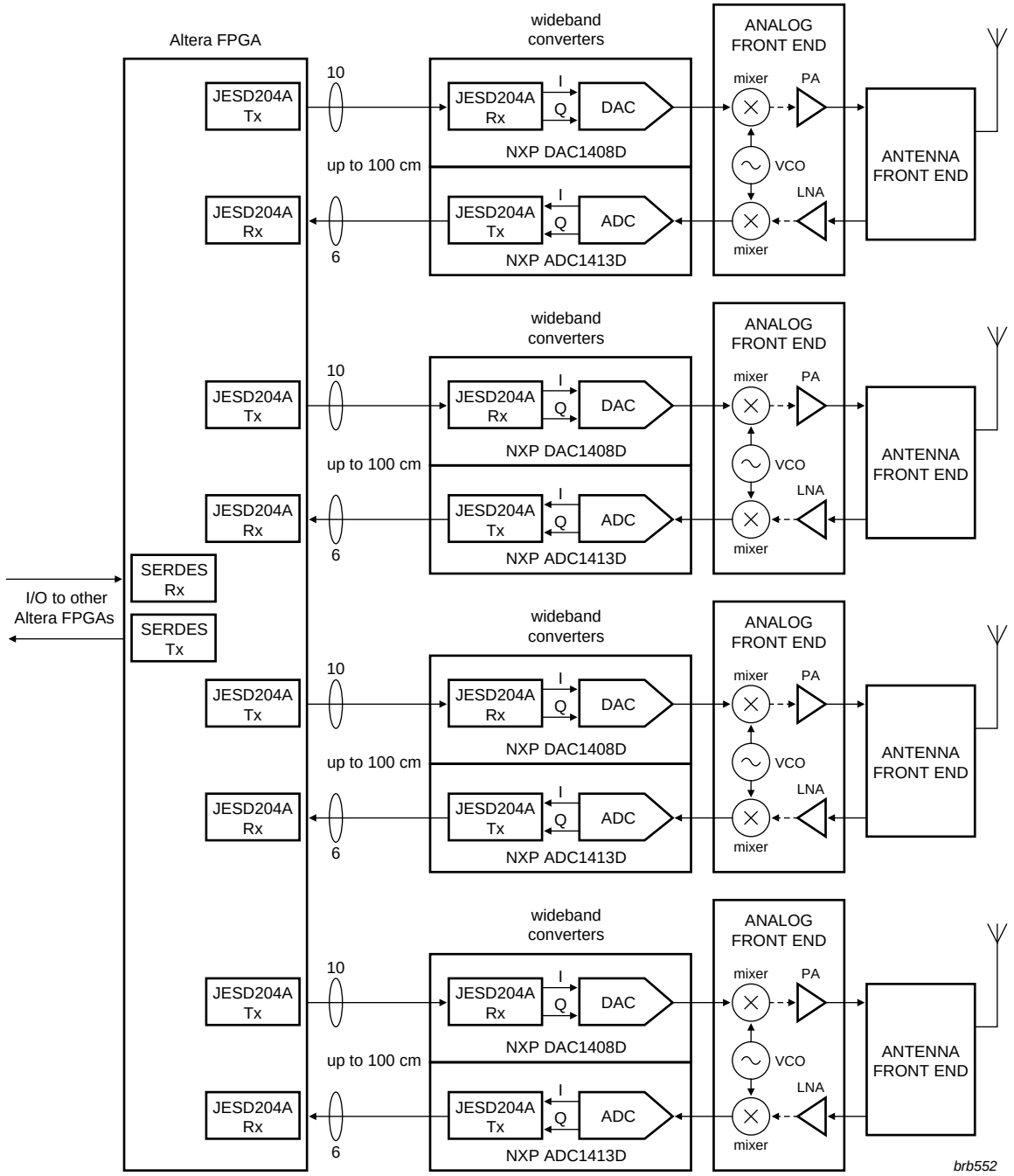

Fig 1. Beam steering system design - JESD204A 14-bit converters

Figure 2 shows some of the shortcomings of phased array systems using traditional parallel interconnections between the sensor data converters and the system DSP resources. The short physical distance afforded by conventional parallel interfaces severely constrains the mechanical form factor of the equipment design.

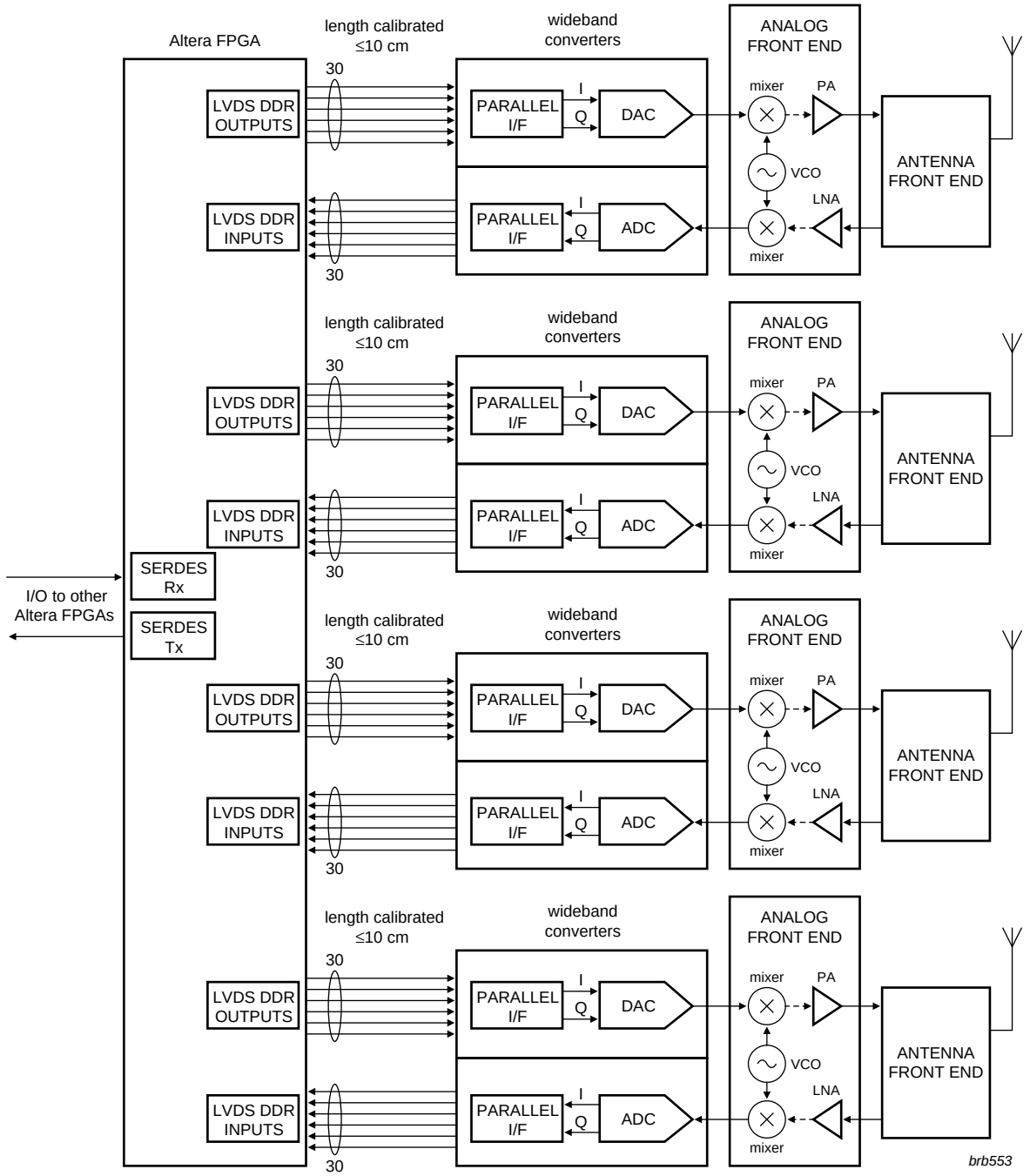

Fig 2. Beam steering system design - LVDS DDR 14-bit converters

5.0 Conclusion – SERDES-based interfaces: inevitable in next generation radars and radios?

Before the availability of JESD204A interface high-speed data converters, traditional parallel interfaces, such as LVCMOS and LVDS DDR, imposed severe PCB layout constraints, making antenna array system design problematic. These conventional interfaces required the interconnecting wiring length to be short and precisely calibrated to avoid signal skew and clocking errors. This required the associated data processor (microprocessor, DSP, FPGA, ASIC) to be located in close proximity to the data converter, severely constraining system design flexibility. With the long reach of JESD204A, combined with the high bandwidth of this standard (312.5 Mbit/s) and the ease-of-use of assured interoperability, beam forming/steering digital communications systems are now practical, cost-effective and destined to become ubiquitous.

A JEDEC JC-16 task group is currently working on the JESD204B specification. This specification revision is expected to increase the maximum serial lane bandwidth to 6.25 Gbit/s or possibly 10 Gbit/s, and add deterministic latency and harmonic frame clocking capabilities (supporting interpolating DACs) to this exciting new interface standard. These enhancements will only increase the attractiveness of this new interface in AESA radar and active antenna array BTS system designs.

While high-speed serial interfaces for data converters have been relatively late to arrive, compared to other high-speed serial interconnects such as USB 2.0 High Speed, PCI Express and Serial ATA, many industry observers see the broad adoption of the JESD204A interface as inevitable. The merits of this interface in digital communication systems such as phased array systems help to understand this perspective.

6.0 Resources – JESD204A technical information

Altera and NXP Semiconductors offer a wealth of technical information on JESD204A for design engineers and system engineers:

http://www.altera.com/literature/po/ss-radioheadapps.pdf

http://www.altera.com/technology/high_speed/protocols/all-protocols/hs-all-protocols.html

http://www.nxp.com/campaigns/fasttrackyourdesign/

There is also a Wikipedia page on JESD204A:

http://en.wikipedia.org/wiki/JESD204

In collaboration with Altera, NXP Semiconductors offers an ADC demonstration board with HSMC connector to enable easy evaluation with Stratix, Arria and Cyclone FPGA development boards. Figure 3 shows the NXP Semiconductors' ADC1613D125WO/DB interfaced with Altera Arria II GX development board for JESD204A interoperability and customer application development.

Fig 3. NXP ADC1613D125WO/DB interfaced with Altera Arria II GX development board

Table 2. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
ASSP	Application Specific Signal Processor
ATA	Advanced Technology Attachment
CGV	Convertisseur Grande Vitesse
DAC	Digital-to-Analog Converter
FLOPS	FLoating-point Operations Per-Second
FPGA	Field-Programmable Gate Array
HSMC	High Speed Mezzanine Card
IP	Intellectual Property
LNA	Low Noise Amplifier
LTE	Long-Term Evolution
LVCMOS	Low-Voltage Complementary Metal-Oxide Semiconductor
LVDS DDR	Low-Voltage Differential Signaling Double Data Rate
NRE	Non-Recurring Engineering
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PCI	Peripheral Component Interconnect
SERDES	SERializer/DESerializer
USB	Universal Serial Bus
WiMAX	Worldwide interoperability for Microwave Access

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